Patent Abstracts of Japan

PUBLICATION NUMBER : 2003023152
PUBLICATION DATE : 24-01-03

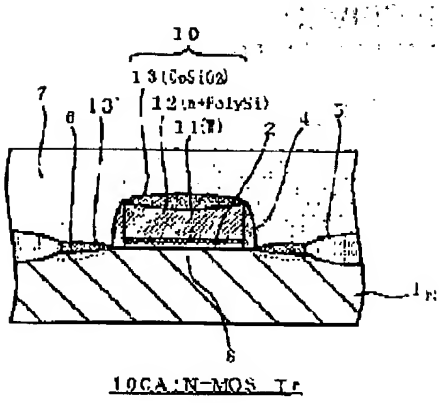
APPLICATION DATE : 10-07-01
APPLICATION NUMBER : 2001209301

APPLICANT : SONY CORP;

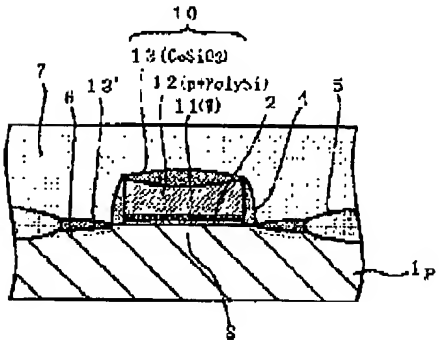
INVENTOR : SUZUKI TOSHIHARU;

INT.CL. : H01L 29/78 H01L 21/285 H01L 29/43
H01L 29/786 // C23C 16/06

TITLE : MIS TRANSISTOR AND METHOD FOR MANUFACTURING THE SAME



10CA:N-MOS Tr



10CB:P-MOS Tr

ABSTRACT : PROBLEM TO BE SOLVED: To freely and continuously control a work function viewed from the gate insulating film side of a gate electrode to a value different from the characteristic value of the materials of the gate electrode, and to continuously control Vth in an MIS type transistor.

SOLUTION: In MIS transistors 100A and 100B, a gate electrode 10 is formed like the laminated configuration of a plurality of kinds of metallic layers 11, 12, and 13 whose work functions are different, and the first metallic layer 11 brought into contact with the gate insulating film 2 is formed with not more than film thickness of 5 Debye length by an atomic layer CVD.

JP2003023152A **2003-1-24**

Bibliographic Fields

Document Identity

(19) 発行国・
日本国特許庁・・・・
(12) 公報種別・
公開特許公報・・・
(11) 公開番号・
特開・・・・・・・・・・・・・・・・・・・・・・
(43) 公開日・
平成・・年・月・・日・・・・・・・・・・

Public Availability

(43) 公開日・
平成・・年・月・・日・・・・・・・・・・

Technical

(54) 発明・名称・
・・型・・・・・・及・・・製造方法
(51) 国際特許分類第７版・
H01L 29/78
21/285
29/43
29/786
// C23C 16/06
FI・
H01L 21/285 C
C23C 16/06
H01L 29/78 301 G
617 L
617 J
617 M
29/62 G
請求項・数・
・
出願形態・
・・

(19) [Publication Office]
Japan Patent Office (JP)
(12) [Kind of Document]
Unexamined Patent Publication (A)
(11) [Publication Number of Unexamined Application]
Japan Unexamined Patent Publication 2003-23152 (P2003-23152A)
(43) [Publication Date of Unexamined Application]
Heisei 15*January 24* (2003.1.24)

(43) [Publication Date of Unexamined Application]
Heisei 15*January 24* (2003.1.24)

(54) [Title of Invention]
MIS TYPE TRANSISTOR AND ITS MANUFACTURING METHOD
(51) [International Patent Classification, 7th Edition]
H01L 29/78
21/285
29/43
29/786
// C23C 16/06
[FI]
H01L 21/285 C
C23C 16/06
H01L 29/78 301 G
617 L
617 J
617 M
29/62 G
[Number of Claims]
4
[Form of Application]
OL

JP2003023152A 2003-1-24

･全頁数･	[Number of Pages in Document]
･	7
･･･････(参考)･	[Theme Code (For Reference)]
4K0304M1045F1105F140	4K0304M1045F1105F140
････(参考)･	[F Term (For Reference)]
4K030 AA02 AA11 BA01 BA05 BA12 BA17 BA18 BA20 BA22 BA29 BB11 BB12 LA15 4M104 AA01 AA09 BB13 BB14 BB16 BB17 BB18 BB40 CC05 DD04 DD43 DD45 DD72 DD84 DD91 EE03 EE09 EE14 EE16 FF13 FF14 GG09 HH20 5F110 AA08 BB04 CC02 DD05 DD13 EE02 EE04 EE14 EE15 EE45 FF01 FF02 FF04 GG02 GG12 NN62 NN66 5F140 AA00 AA06 AB03 AC36 BA01 BD09 BD11 BD12 BF07 BF11 BF14 BF15 BF17 BF21 BF28 BG08 BG28 BG34 BK21 BK34 CB01 CB08 CF04	4K030 AA02 AA11 BA 01 BA 05 BA 12 BA 17 BA 18 BA 20 BA 22 BA 29 BB11 BB12 LA15 4M104 AA01 AA09 BB13 BB14 BB16 BB17 BB18 BB40 CC05 DD04 DD43 DD45 DD72 DD84 DD91 EE03 EE09 EE14 EE16 FF 13 FF 14 GG09 HH20 5F110 AA08 BB04 CC02 DD05 DD13 EE02 EE04 EE14 EE15 EE45 FF 01 FF 02 FF 04 GG02 GG12 NN62 NN66 5F140 AA00 AA06 AB03 AC36 BA 01 BD09 BD11 BD12 BF07 BF11 BF14 BF15 BF17 BF21 BF28 BG08 BG28 BG34 BK21 BK34 CB01 CB08 CF04
Filing	
･審査請求･	[Request for Examination]
未請求	Unrequested
(21) ･出願番号･	(21) [Application Number]
特願･････ ･･･････････････ ･･････	Japan Patent Application 2001-209301 (P2001-209301)
(22) ･出願日･	(22) [Application Date]
平成･･年･月･･日 ･･････････	Heisei 13*July 10* (2001.7.10)
Parties	
Applicants	
(71) ･出願人･	(71) [Applicant]
･識別番号･	[Identification Number]
･････････	000002185
･氏名又･名称･	[Name]
･･･株式会社	**SONY CORPORATION (DB 69-055-3649)**
･住所又･居所･	[Address]
東京都品川区北品川･丁目･番･･号	Tokyo Shinagawa-ku Kitashinagawa 6-7-35
Inventors	
(72) ･発明者･	(72) [Inventor]
･氏名･	[Name]
小松 裕司	Komatsu Yuji
･住所又･居所･	[Address]
東京都品川区北品川･丁目･番･･号 ･･･株式会社内	Tokyo Shinagawa-ku Kitashinagawa 6-7-35 Sony Corporation (DB 69-055-3649) *

JP2003023152A 2003-1-24

(72) 発明者・

氏名・

鈴木 俊治

住所又・居所・

東京都品川区北品川・丁目・番・・号 ・・・株式会社内

Agents

(74) 代理人・

識別番号・

・・・・・・・・・

弁理士・

氏名又・名称・

田治米 登 外・名・

Abstract

(57) 要約・

課題・

MIS 型・・・・・・・・・・・・・・電極・・・絶縁膜側・・見・仕事関数・・・・・・・電極・材料・・・特性値・・異・・値・自由・連続的・制御・・・・・・・・ Vth ・連続的・制御・・・

解決手段・

MIS 型・・・・・・ 100A・100B ・・・・・・・・電極 10 ・・仕事関数・異・・複数種・金属層 11・12・13 ・積層構造・・・・・・・・・絶縁膜 2 ・接・・第 1 ・金属層 11 ・・原子層 CVD ・・・・膜厚 5 ・・・ ・長以下・形成・・・

(72) [Inventor]

[Name]

Suzuki Toshiharu

[Address]

Tokyo Shinagawa-ku Kitashinagawa 6-7-35 Sony Corporation (DB 69-055-3649) *

(74) [Attorney(s) Representing All Applicants]

[Identification Number]

100095588

[Patent Attorney]

[Name]

Tajime * (1 other)

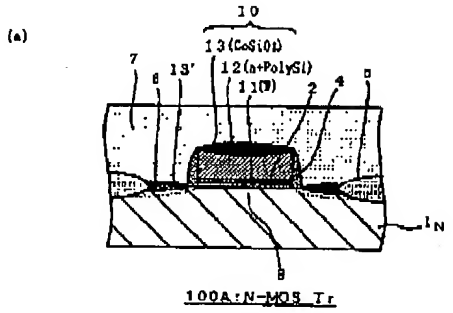
(57) [Abstract]

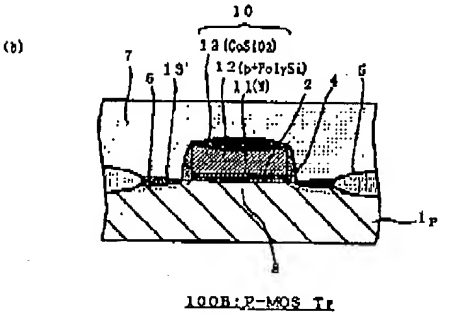
[Problems to be Solved by the Invention]

In MIS type transistor , characteristic value where material of gate electrode has work function which was seen from gate insulating film side of gate electrode , in value whichdiffers it controls freely in continuous , it controls Vth in the continuous with that.

[Means to Solve the Problems]

In MIS type transistor 100A, 100B, it designates gate electrode 10, as laminated structure of metal layer 11, 12, 13 of multiple kinds where work function differs, it forms below film thickness 5debye length the first metal layer 11 which at same time touches to gate insulating film 2, with atomic layer CVD .





Claims

特許請求・範囲・

請求項 1・

・・・電極・・仕事関数・異・・複数種・金属層・積層構造・有・・・・・・・絶縁膜・接・・第 1 ・金属層・・原子層 CVD(Atomic Layer Chemical Vapour Deposition: ALCVD)・・・・膜厚 5 ・・・長以下・形成・・・・・・・・特徴・・・MIS 型・・・・・・・

請求項 2・

第 1 ・金属層・膜厚・0.6・・・長以上・・・請求項 1 記載・MIS 型・・・・・・・

請求項 3・

・・・電極材料・積層・・・・・電極・形成・・MIS 型・・・・・・・製造方法・・・・・・・電極材料・・・・・・第 1 ・金属層・・・・絶縁膜上・原子層 CVD ・・・膜厚 5 ・・・長以下・形成・・・・上・第 1 ・金属層・異・・金属種・第 2 ・金属層・積層・・・・・特徴・・・MIS 型・・・・・・・製造方法・

請求項 4・

第 1 ・金属層・膜厚 0.6・・・長以上・形成・

[Claim(s)]

[Claim 1]

first metal layer where gate electrode , has laminated structure of metal layer of multiple kinds where work function differs, at same time touches to gate insulating film , the MIS type transistor . which designates that it is formed below film thickness 5debye length by the atomic layer CVD (Atomic Layer Chemical Vapour deposition : ALCVD), as feature

[Claim 2]

MIS type transistor . which is stated in Claim 1 where film thickness of first metal layer is0.6 debye lengths or more

[Claim 3]

manufacturing method . of MIS type transistor which designates that second metal layer of metal type where first on gate insulating film forms first metal layer below film thickness 5debye length with the atomic layer CVD . it laminates gate electrode material , in manufacturing method of MIS type transistor which forms gate electrode , as gate electrode material , differs from first metal layer on that is laminatedas feature

[Claim 4]

manufacturing method . of MIS type transistor which is stated

・請求項3記載・MIS型・・・・・・・製造方法・

in Claim 3 which forms the first metal layer above film thickness 0.6debye length

Specification

・発明・詳細・説明・

[Description of the Invention]

・0001・

[0001]

・発明・属・・技術分野・

[Technological Field of Invention]

本発明・・半導体/絶縁膜/金属・積層構造・有・・MIS型・・・・・・・・・・・・・絶縁膜側・・見・・・・電極・仕事関数・連続的・制御・・・・・・・・・・・・・・・・・閾値Vth・制御・・技術・関・・・

It tries this invention, to be able to control work function of gate electrode whichwas seen from gate insulating film side in MIS type transistor which possesses laminated structure of the semiconductor /insulating film /metal , in continuous , technology which controls threshold value Vth of transistor with that it regards.

・0002・

[0002]

・従来・技術・

[Prior Art]

・・・Si基板・形成・・・MIS型・・・・・・・・図4(a)・(b)・示・N-MOS・・・・・・・P-MOS・・・・・・・・・・・一般・Si基板・N・・・l_N又・P・・・l_P上・・・絶縁膜2・形成・・・・絶縁膜2上・・・・n+PolySi又・p+PolySi・・・・・・電極3_N・3_P・積層・・構造・有・・・・・

MIS type transistor which was formed to bulk Sisubstrate , Figure 4 (a), like N- MOS transistor , P-MOS transistor which is shown in (b), generally, forms gate insulating film 2 in Nwell 1_N of Sisubstrate , or on Pwell 1_P furthermore has possessed structure whichlaminates gate electrode 3_N, 3_P which consists of n+PolySi or p+PolySi on the gate insulating film 2.

・・・図中・符号4・・・・電極・・・・・・・・・・符号5・LOCOS・・・素子分離膜・・・符号6・拡張・・・又・拡張・・・・領域・・・・符号7・層間絶縁膜・・・・

Furthermore, as for in the diagram , sign 4 with sidewall of gate electrode , as for the sign 5 with element-isolating film , as for sign 6 with extended source or theextended drain region , as for sign 7 it is a interlayer insulating film with LOCOS .

・0003・

[0003]

従来・・・・・・・・・・閾値Vth・・・・・・部8・不純物濃度・・・・制御・・・・・・

Until recently, threshold value Vth of this transistor is controlled with impurity concentration of channel part 8.

・・・・部8・不純物濃度制御・・0.18μm程度・・・・・・・・・LSI・・・・・・・注入技術・短時間熱処理技術・・駆使・・比較的良好・行・・・・・・

impurity density control of channel part 8, freely using ion implantation technology and short time thermal processing technology , is donerelatively satisfactorily to LSI of design rule of 0.18:mu m extent .

・0004・

[0004]

・・・・・0.1μm・・・・・・以降・・・・・・・・・・・・・・・・・・・・・・・・・・・・・不純物量・・・Vth・制御・・手法・・・・・・・長・短・・・・・・・・1個当・・・・・・・・・・・・Vth・寄与・・不純物・絶対数・少・・・・統計的・・・・・・・Vth・・・・・・無視・・・・・・・・・・(T.Mizuno et al, "Performance Fluctuations of 0.10 μm MOSFETs - Limitationof 0.1 μm ULSIs"等, Symp. on VLSI Technology '94)・

However, regarding 0.1;mu m or design rule transistor of after that,with technique which controls Vth with amount of impurity of channel ,as channel length becomes short, absolute number of impurity which contributesto Vth of transistor of per each decreases, It has become not be able to ignore variation of Vth with thestatistical fluctuation , (Symp. on VLSI technology '94 such as T.Mizuno et al. "Performance Fluctuations of 0.1 0 ;mu m MOSFETs - Limitationof 0.1 ;mu m ULSIs").

・・・・・・・部・不純物濃度制御・他・・・・電極・仕事関数・・・・・・・・・・・・・・・Vth ・制御・・・・・・・・・・・・微細・・・・対応・・・・・・・・切望・・・・・・・・・・・

0005・

一方・SOI(Silicon on Insulator)基板・用・・・・・・・・・・活性 SOI 層・数十 nm ・薄・・・・0.25μm 程度・・・・・・・・・・・・・・不純物濃度制御・・・Vth ・制御・・原理的・限界・・・・

・・・・・・・部・不純物濃度・・例・・ 1×$10^{18}cm^{-3}$ 以上・高濃度・・・・・不純物散乱・増大・伴・・・・・・移動度・低下・・・・・電流駆動能力・低下・・・・・Vth ・ SOI ・膜厚依存性・増大・無視・・・・・・・・好・・・・・

・・・・SOI 基板・用・・・・・・・・・・・・・・・・電極・仕事関数・・・・・・・・・・・Vth ・制御・・・・・切望・・・・・・

0006・

・・他・・・・電極・低抵抗化・・・・電極・空乏化防止等・・・・・・電極・金属・形成・・・・・必要・・・・・・・・・・・・・・・・・・Vth ・・・・電極・仕事関数・制御・・・・制御・・・・・・望・・・・・・

0007・

発明・解決・・・・・・課題・

・・・・・・・・・・電極・材料・決・・・・・・・・・・・閾値 Vth ・・・・・・・・・・・・構造(・・・・不純物濃度・・・・絶縁膜・膜厚等)・・・・必然的・決・・・・・・・・電極・単・金属・形成・・場合・・一種類・ Vth ・有・・・・・・・・・・作製・・・・・・・・・・問題・・・・

0008・

・・・対・・・・・・電極・材料・・・多結晶 TiN ・配向性・変化・・・同・材料・用・・・・・仕事関数・種・・値・制御・・試・・行・・・・・(K.Nakajima et al, 1999 Symposium on VLSI Technology Digest of Technical Papers, p95(1999))・

・・・・・・・・・手法・・・制御・・・仕事関数・範囲・・基本的・結晶方位・・・仕事関数・差・範囲内(通常・0.1V 程度・・)・制限・

Then, other than impurity density control of channel part , to try to be able to control Vth of transistor even with work function of gate electrode . as process of fine device correspondence it is designed in such a way that it isdesired.

[0005]

On one hand, because with transistor which uses SOI (silicon-on-insulator) substrate , the activity SOI layer several tens of nm is thin, regarding design rule of 0.25;mu m extent . with impurity density control in control of Vth there is a limit in principle .

In addition, when impurity concentration of channel part , is designated as high concentration above for example 1X 10¹⁸cm ⁻³, because mobility of carrier decreases attendantupon increase of impurity scattering , because current drive capacity can decrease,furthermore, cannot ignore increase of film thickness dependency of SOI of Vth and becomes it is not desirable.

Then, regarding transistor which uses SOI substrate , it is desired that the Vth of transistor is controlled with work function of gate electrode .

[0006]

Because of depletion prevention or other of resistance-lowering , gate electrode of this otherthings and gate electrode , it is designed in such a way that is needed that gate electrode is formed with metal , it is desired Vth evenbecause of that that it controls with control of work function of the gate electrode .

[0007]

[Problems to be Solved by the Invention]

But, when material of gate electrode is decided, because threshold value Vth of the transistor is decided inevitably with device structure (film thickness etc of channel impurity concentration , gate insulating film) of transistor , when the gate electrode is formed simply with metal , there is a problem that only the transistor which possesses Vth of one kind it is possible toproduce.

[0008]

K.Nakajima et al, 1999 symposium on VLSI technology Digest of Technical Papers , p95 (1999). orientation of polycrystalline TiN changing vis-a-vis this, as material of the gate electrode , making use of same material although, attempt whichcontrols work function in various value being done, it is

But, because with this technique , range of work function which can becontrolled, in basic to (Usually, to 0.1 Vextent) inside range of difference of the work function is restricted

・・・・・仕事関数・連続的・制御・・・・・・・・・・原理的・課題・・・・・・多結晶・配向・100%制御・・・・不可能・近・・・微細・・・・・・・・応用・考・・場合・・再現性・歩留・・・点・・・課題・多・・

0009・

・・本発明者・・・・酸化膜上・・・・電極・・・・・・CVD 法・・・・・等・・・島状領域・形成・・次・・島状領域上・・・島状領域・構成材料・・異・・材料・薄膜・積層・・・・場合・島状領域・薄膜・・・・酸化膜・対・・被覆率等・変化・・・・・・・・・・電極・仕事関数・変化・・・手法・提案・・・(特開平 7-211896 号公報)・

・・・・・・・・手法・・・・・・・・微細化・伴・・島状領域・被覆率・・1・・・・・・内・平均化・・・・特性・・・・・・増大・・・・問題・・・・

0010・

以上・・・・従来技術・対・・本発明・・MIS 型・・・・・・・・・・・・・電極・・・・絶縁膜側・・見・仕事関数・・・・・・電極・材料・・・特性値・・異・・値・自由・連続的・制御・・・・・・・Vth ・連続的・制御・・・・・・・・・・・目的・・・・

0011・

課題・解決・・・・・手段・

本発明者・・・仕事関数・異・・複数種・金属・積層膜・用・・MIS 型・・・・・・・・・電極・形成・・場合・・・・絶縁膜・接・・第 1 ・金属層・膜厚・5・・・長(即・・数原子層)以下・薄・形成・・・・上・第 2 ・金属層・積層・・・・・・絶縁膜側・・見・実効的・仕事関数・・第 1 ・金属層・固有・仕事関数・第 2 ・金属層・固有・仕事関数・・問・連続的・制御・・・・・・・場合・第 1 ・金属層・原子層 CVD(Atomic Layer Chemical Vapour Deposition: ALCVD)・・・形成・・・・5 ・・・長以下・・・薄膜・・・・・所定・膜厚・再現性・・安定的・形成・・・・・・見出・・・

0012・

即・・本発明・・・・・電極・・仕事関数・異・・複数種・金属層・積層構造・有・・・・・・絶縁膜・接・・第 1 ・金属層・・原子層 CVD ・・・・膜厚 5 ・・・長以下・形成・・・・・・・・特徴・・・MIS 型・・・・・・・・提供

with crystal orientation , there to be a principle problem that, it isnot possible to control work function in continuous , in addition, becausething which orientation of polycrystalline 100% is controlled is closeto impossible , when of application to microscopic transistor was thought, problem is many even from point of reproducibility and yield .

[0009]

In addition, in this inventor on gate oxide film , first forming island region whichconsists of silicon etc with CVD method as gate electrode , next,laminating thin film with material which constituent material of island region differs on island region , island region in this case and coating ratio etc for gate oxide film of thin film changing depending, work function of gate electrode technique which changes is proposed, (Japan Unexamined Patent Publication Hei 7-211896disclosure).

But, in this technique , coating ratio of island region , averaging is not doneinside device of one attendant upon narrowing of device ,there is a problem that variation of characteristic increases.

[0010]

Like above vis-a-vis Prior Art , characteristic value where material of gate electrode has work function which was seen from gate insulating film side of gate electrode in the MIS type transistor , in value which differs it controls this invention, freely in the continuous , it designates that it tries to be able to control Vth in continuous with that as objective .

[0011]

[Means to Solve the Problems]

When when gate electrode of MIS type transistor is formed making use of laminated film of metal of multiple kinds where work function differs, film thickness of first metal layer which touches with gate insulating film it forms these inventors , thin 5 debye long (Namely, several atomic layers),or less laminates second metal layer on that, effective work function which was seen from gate insulating film side, In first metal layer in work function and second metal layer of peculiar between work function of peculiar it can control in continuous , in case of this , when first metal layer is formed with atomic layer CVD (Atomic Layer Chemical Vapour deposition : ALCVD), even with thin film , 5 debye lengths or less fact that reproducibility well it can form in stable was discovered in predetermined film thickness .

[0012]

Namely, as for this invention, gate electrode , has laminated structure of metal layer of the multiple kinds where work function differs, first metal layer which at same timetouches to gate insulating film , offers MIS type transistor which designates that it isformed below film thickness 5debye length

・・・

'0013・

・・・本発明・・・・・絶縁膜上・・・・電極材料・積層・・・・・電極・形成・・・MIS 型・・・・・・・製造方法・・・・・・・電極材料・・・・・・第 1 ・金属層・・・・絶縁膜上・原子層 CVD ・・・膜厚 5 ・・・長以下・形成・・・・上・第 1 ・金属層・異・・金属種・第 2 ・金属層・積層・・・・・特徴・・・MIS 型・・・・・・・製造方法・提供・・・

by atomic layer CVD , as feature.

[0013]

In addition, first on gate insulating film forms first metal layer below film thickness 5debye lengthwith atomic layer CVD , this invention laminates gate electrode material on gate insulating film , in the manufacturing method of MIS type transistor which forms gate electrode , as gate electrode material , offers the manufacturing method of MIS type transistor which designates that second metal layer of metal type whichdiffers from first metal layer on that is laminated as feature.

'0014・

・発明・実施・形態・

以下・図面・参照・・・・本発明・詳細・説明・・・

・・・各図中・同一符号・同一又・同等・構成要素・表・・・・・

[0014]

[Embodiment of the Invention]

While below, referring to drawing , you explain this invention in detail.

Furthermore, each in the diagram , same sign has displayed same or equal component .

'0015・

図 1(a)・(b)・・・・・・本発明・MIS 型・・・・・・・一実施形態・示・ N-MOS 又・P-MOS ・・・・・・ 100A・100B ・模式的断面図・・・・

[0015]

Figure 1 (a), (b) is schematic sectional view of N- MOS or P-MOS transistor 100A, 100B whichshows one embodiment of MIS type transistor of respective this invention .

・・・・・・・100A・100B ・・・・・Si 基板・N ・・・ 1_N又・P ・・・ 1_P上・SiO_2・・・・・・絶縁膜 2 上・形成・・・・・電極 10 ・・・・絶縁膜 2 側・・・・・・・・・(W)・・・・第 1 ・金属層 11 ・・n+PolySi 又・p+PolySi ・・・・第 2 ・金属層 12 ・・$CoSi_2$・・・・第 3 ・金属層 13 ・積層構造・有・・・・・

As for this transistor 100A, 100B, gate electrode 10 which was formed on gate insulating film 2 whichconsists of Nwell 1_N of bulk Sisubstrate or SiO₂ on Pwell 1_P, from gate insulating film 2 side, has had laminated structure of metal layer 13 of 3 rd which consist of second metal layer 12 and CoSi₂ which consist of first metal layer 11 and n+PolySi or p+PolySi which consist of [tansuguten] (W).

・・・図中・符号 13'・・第 3 ・金属層 13 ・同種・金属・拡張・・・又・拡張・・・・領域 6 上・形成・・金属層・・・・

Furthermore, in the diagram , sign 13' is extended source or metal layer which wasformed on extended drain region 6 with metal layer 13 of 3 rd and metal of same kind .

'0016・

・・・・第 1 ・金属層 11 ・・膜厚 0.6 ・・・長~5 ・・・長(即・・0.1 原子層~数原子層)・形成・・・・・・

[0016]

Here, first metal layer 11 is formed to film thickness 0.6debye long - 5 debye long (Namely, 0.1 atomic layer ~several atomic layers).

第 2 ・金属層 12 ・・PolySi ・濃度~$5 \times 10^{20} cm^3$・・・・(P)(N-MOS Tr :100A) 又・・・・素(B)(P-MOS Tr :100B)・・・・・・・・・・・・完全・導電体(n+PolySi 又・p+PolySi)・・・・・・・・膜厚50~300nm ・形成・・・・・・

second metal layer 12 completely conductor (n+PolySi or p+PolySi) with being something which is done phosphorus of concentration ~5X 10²⁰ cm ³ (P) (N- MOS Tr :100A) or by doped doing boron (B) (P-MOS Tr :100B) in PolySi, is formed to film thickness 50~300nm .

・・・第 3 ・金属層 13 ・・10~100nm ・形成・・・・・・

In addition, metal layer 13 of 3 rd is formed to 10 - 100 nm .

'0017・

[0017]

・・・・・・・100A・100B・・・・本発明・・第1・金属層11・膜厚・5・・・長以下・薄・形成・・・・・・・・・・電極10・・・絶縁膜2側・・見・実効的・仕事関数・・第1・金属層11・金属種・・・定・・仕事関数・第2・金属層12・金属種・・・定・・仕事関数・中間・仕事関数・・・・・・・・・値・第1・金属層11・膜厚・・・・連続的・変化・・・所期・値・・・・

Like this transistor 100A, 100B, with this invention , to make work function of intermediate of the work function which becomes settled due to metal type of work function and the second metal layer 12 which become settled effective work function which was seen from gate insulating film 2 side of gate electrode 10 film thickness of first metal layer 11 by forming thin 5 debye lengths or less, due to metal type of first metal layer 11, furthermore, valuewith film thickness of first metal layer 11 changing in continuous . It makes anticipated value.

・・・・・第1・金属層11・膜厚・制御・・・・仕事関数・制御・・・・・・第・金属層11・・・・第2・金属層12・影響・・・・・・・・・・第1・金属層11・膜厚・1・・・長増・・・・・・・・絶縁膜2側・・見・第2・金属層12・影響・1/e・急激・減少・・第1・金属層11・膜厚・5・・・長・超・・・・・絶縁膜2側・・見・仕事関数・・・第2・金属層12・影響・実質的・現・・・・・・・・・(Appl.Phys.Lett.,54(3),p268(1989)参照)・

this way whenever as for being able to control work function withcontrol of film thickness of first metal layer 11, influence of second metal layer 12 because the shield it is done, film thickness of first metal layer 11 1 debye length increases with first metal layer 11 when, influence of second metal layer 12 which was seen from gate insulating film 2 sidedecreases to 1 /e suddenly, film thickness of first metal layer 11 exceeds 5 debye length, in work function which was seen from gate insulating film 2 side, Because influence of second metal layer 12 stops appearing substantially, (Applied Physics Letters , 54 (3), p268 (1989) reference).

・0018・

・・・第1・金属層11・薄・形成・・場合・・第1・金属層11・・1原子層未満・即・・金属原子・連続層・・・・離散的・・互・・重・・合・・・・・・・・絶縁膜上・形成・・・・・・・・

[0018]

Furthermore, when first metal layer 11 is formed thin, first metal layer 11 under 1 atomic layer ,namely, metal atom not to be a continuous layer , to discrete , may be formed on gate insulating film mutually stacking without being agreeable.

・0019・

本発明・・・第1・金属層11・・・・絶縁膜2上・膜厚・原子層・・・・制御・・形成・・・・・・原子層CVD・・第1・金属層11・・構成原子・1層・・・・・・以下・膜厚・・堆積・・・

[0019]

With this invention , in order on gate insulating film 2 controlling film thickness with the atomic layer level , to form first metal layer 11, with atomic layer CVD , it accumulates 1 layer or film thickness of less than that at a time constituent atom of first metal layer 11.

原子層CVD・・従来・MBE(Molecular Beam Epitaxy)・・異・・・必・・・下地・結晶基板・必要・・・・・・・・超高真空・必要・・・・・・・SiO_2等・非晶質・・・・絶縁膜上・制御性・・原子層・・・・薄膜・成長・・・・・・・・・・

As for atomic layer CVD , crystal substrate not to be always done necessity in the substrate conventional MBE (Molecular Beam Epitaxy) unlike, in addition, because either ultrahigh vacuum isnot needed, on gate insulating film of SiO₂ or other amorphous controlability thin film it can growwell with atomic layer level .

・0020・

・・・原子層CVD・・・・・分子(Precursor)・吸着・・・・対・・大・・場合・・・分子・吸着時・未吸着・・・・・・・・・・・・・・・・分子・吸着・・・1・・・・・操作・1原子層・堆積・・・・・・・・・通常・0.1原子層(0.6・・・・長)程度・堆積・・・・・・数・重・・・・・・・1原子層・堆積・・・・・・・・

[0020]

In addition, with atomic layer CVD , when gas molecule (Precursor) it is large vis-a-vis adsorption site , because unadsorbed site mask it is done when adsorbing of gas molecule , gas molecule it is not case that 1 atomic layer accumulates withoperation of 1 cycle which adsorbs, usually, 0.1 atomic layer (0.6 debye length) extent accumulate, means with that 1 atomic layer accumulates by repeating the number of cycles .

・・・・・・・・・数・制御・・・・・・・・・・・的・金属層・膜厚・制御・・・・可能・・・(Surface chemistry of materials deposition at atomic layer level, Tuomo Suntola, Applied Surface Science 100 101, 391-398(1996)参照)・

0021・

本発明・・・・・第1・金属層11・膜厚・下限・・・・・・・・・絶縁膜2側・・見・仕事関数・制御・・点・・・格別制限・・・・

・・・・・原子層 CVD ・被吸着体・・・分子・吸着・・・|・・・・・・・・・被吸着体・堆積・・原子層・膜厚・下限値(通常 0.1 原子層)・・第1・金属層11・膜厚・実際上・下限値・・・・

0022・

第1・金属層11・膜厚・制御・・・・・・・絶縁膜2側・・見・・・・電極10・仕事関数・制御・具体例・・・・・例・・・第1・金属層11・3原子層程度・・・・・・・絶縁膜2・・見・仕事関数・・N-MOS ・・・・・・100A P-MOS ・・・・・・100B 共・・・・・・W 膜・有・・仕事関数Φ_M・4.55eV 程度・・・第1・金属層11・1原子層程度・・・場合・・・・・・絶縁膜2・・見・仕事関数Φ_M・4.55eV ・近・値・・・・・第1・金属層11・膜厚・0.1 原子層程度・・・・・W 原子・・・絶縁膜2・表面・被覆・・被覆率・・・比例・・・・・絶縁膜2側・・見・仕事関数Φ_M・線形的・変化・・・・・・・・N-MOS ・・・・・・100A ・・・W 膜・仕事関数Φ_M・4.1~4.55eV ・制御・・・P-MOS ・・・・・・100B ・・4.55~5.2eV ・制御・・・・

・・・・・・第1・金属層11・膜厚・0.5 原子層程度・・・・・・・・N-MOS ・・・・・・100A ・・仕事関数Φ_M・4.3eV 程度・・・・P-MOS ・・・・・・100B ・・仕事関数Φ_M・4.9eV 程度・・・・・

0023・

本発明・・・・・第2・金属層12・・上述・・・・・・100A 100B ・・・・・・・・絶縁膜2側・・見・仕事関数・・第3・金属層13・影響・現・・・・・・厚・形成・・・・・・・必要・応・・・・・・絶縁膜2側・・見・仕事関数・・第1・金属層11・第2・金属層12・・・・・第3・金属層13・影響・現・・・・・

Therefore, by fact that number of cycles is controlled, it becomespossible to control film thickness of metal layer in digital , (Surface chemistry of materials deposition ata tomic layer level , Tuomo Suntola, Applied Surface Science 100/101, 391-398 (1996) reference).

[0021]

Regarding to this invention, there is not exception restriction from thepoint which controls work function which you saw from gate insulating film 2 sideconcerning lower limit of film thickness of first metal layer 11.

Because of this , with 1 cycle which gas molecule adsorbs into thesuffering adsorbant with atomic layer CVD , lower limit (Usually, 0.1 atomic layer) of film thickness of atomic layer which is accumulated in suffering adsorbant , becomes really lower limit on film thickness of first metal layer 11.

[0022]

When with control of film thickness of first metal layer 11, for example first metal layer 11 is designatedas 3 atomic layer extent as embodiment of control of work function of gate electrode 10 which wasseen from gate insulating film 2 side, even with when work function which was seen from the gate insulating film 2 both N- MOS transistor 100A, P-MOS transistor 100B. becomes 4.55 eV extent of work function :ph _M which W film of bulk has, designates first metal layer 11 as 1 atomic layer extent , work function :ph _M which was seen from gate insulating film 2 reaches valuewhich is close to 4.55 eV , but when film thickness of first metal layer 11 isdesignated as 0.1 atomic layer extent , Watom almost being proportionate to the coating ratio which surface of gate insulating film 2 sheath is done, work function :ph_M which was seen from gate insulating film 2 side it to be possible to change in linear , with N- MOS transistor 100A, Be able to control work function :ph _M of W film in 4.1 - 4.55 eV , it can control with P-MOS transistor 100B in 4.55 - 5.2 eV .

Therefore, it depends on designating film thickness of first metal layer 11 as 0.5 atomic layer extent , work function :ph _M can designate with N- MOS transistor 100A as 4.3 eV extent ,with P-MOS transistor 100B can designate work function :ph _M as 4.9 eV extent .

[0023]

Regarding to this invention, like above-mentioned transistor 100A, 100B, in order in work function which was seen from gate insulating film 2 side, for influence of metal layer 13 of 3 rd not to appear, it is possible to form second metal layer 12, thickly,but in work function which was seen from according to need , gate insulating film 2 side, it is possible notonly a first metal layer 11 and a second metal layer 12, that influence

・・・・・

・・場合・・・第 2 ・金属層 12 ・・原子層 CVD ・数原子層以下・形成・・・

【0024】

第 3 ・金属層 13 ・・・・・電極 10 ・低抵抗化・・・・・・・・・・・注入時・注入・・不純物・・・・下・注入・・・・・・・・・・・・・・・・・形成時・・・・・・・・・・・等・・・・必要・応・・設・・・・・

【0025】

本発明・ MIS 型・・・・・・・・製造方法・・・・・上述・・・・第 1 ・金属層 11 ・原子層 CVD ・形成・・以外・公知・方法・・・・・・・・・例・・・図 1(a)・ N-MOS ・・・・・・ 100A ・・図 2 ・示・・・・製造・・・・・・・・・

【0026】

(1)・・・・・・ Si 基板 14 ・・公知・手法・LOCOS 法・・・素子分離膜 5 ・N ・・・ 1_N ・形成・・(図 2(a))・

【0027】

(2)次・・・・・絶縁膜2 ・・・ SiO_2 ・・例・・1.5~4.0nm 程度成長・・・(図 2(b))・

【0028】

(3)・・・絶縁膜 2 上・・原子層 CVD ・・・・第 1 ・金属層 11 ・・・ W 膜・膜厚 0.6 ・・・長~5 ・・・長(即・・0.1 原子層~数原子層)堆積・・(図 2(c))・

・・場合・原子層 CVD 条件・・例・・・基板温度・300 deg C ・・・・・分子(Precursor)・・・・ $WOCl_4$ ・使用・・・・・・・・・・・・・・・・・・・・・ $WOCl_4$ 流入 ・N_2 排気 ・H_2 流入 ・N_2 排気・工程・繰・返・・

【0029】

(4)第 1 ・金属層 11(W 膜)上・・PolySi ・通常・ CVD ・・・膜厚 50~300nm 堆積・・・・・・N-MOS ・・・・・・・形成領域・・ P ・・・・・例・・・20keV ・濃度 $5\times10^{15}cm^{-2}$ ・・・・・・打・込・・ n+PolySi ・形成・・・・・第 2 ・金属層 12 ・・・(図 2(d))・

・・・P-MOS ・・・・・・・形成・・場合・・・形成領域・・ B ・・・・・例・・加速電圧

of metal layer 13 of 3 rd appears.

In that case, with atomic layer CVD it forms also second metal layer 12. below several atomic layers .

[0024]

metal layer 13 of 3 rd , as for sake of of resistance-lowering of gate electrode 10 or according to need is provided etching stopper etc at time of mask , contact formationwhich impurity which is filled at time of ion implantation tries is notfilled that under gate .

[0025]

As manufacturing method of MIS type transistor of this invention , above-mentioned way otherthan forming first metal layer 11 with atomic layer CVD , it can do thing with known method .as shown in Figure 2 , it can produce N- MOS transistor 100A of for example Figure 1 (a).

[0026]

(1) First, in bulk Sisubstrate 14, with technique of public knowledge element-isolating film 5 and the Nwell 1_N are formed with LOCOS method (Figure 2 (a)).

[0027]

(2) Next, SiO₂ , for example 1.5~4.0nm extent it grows as gate insulating film 2.(Figure 2 (b)).

[0028]

Figure 2 (c). On (3) gate insulating film 2, W film film thickness 0.6debye long - 5 debye long (Namely, 0.1 atomic layer ~several atomic layers) isaccumulated with atomic layer CVD , as first metal layer 11

In case of this , atomic layer CVD condition designates for example substrate temperature as 300 deg C,uses WOCl<sub>4< sub> gas molecule (Precursor) as, WOCl<sub>4< sub> influx, N₂exhaust , H₂ influx and the N₂exhaust repeats step gas [furooshiikuuensu] as.

[0029]

Figure 2 (d). On (4) first metal layer 11 (W film), film thickness 50~300nm it accumulates PolySi with conventional CVD ,in order furthermore, in forming region of N- MOS transistor Pion . to become concentration 5X 10¹⁵cm ⁻² with for example 20keV , ramming down, it forms n+PolySi, this the second metal layer 12 does

Furthermore, when P-MOS transistor is formed, in order Bion , with the for example acceleration voltage 10keV , to

10keV ・ ・濃度 5×10^{15}cm^{-2} ・・・・・・打・込・・ p+PolySi ・形成・・・

N-MOS ・・・・・・・形成領域・P-MOS ・・・・・・・形成領域・・・・・・打・分・・・・・・・・・・・15 ・用・・・

0030・

(5)・・後・公知・手法・・・・・・電極 10 ・・・・・・形成・・拡張・・・又・拡張・・・・領域 6 ・不純物・注入・・・・・電極 10 ・・・・・・・・4 ・形成・・・・・S 及・・・・・D ・・不純物・注入・活性化・行・・CoSi$_2$ ・・・金属層 13 ・13'・第 2 ・金属層 12 上及・拡張・・・又・・・・・領域 6 上・自己整合的・形成・・層間絶縁膜 7 ・堆積・(図 2(e))・・・・・・・・・・形成・・・・・充填・配線・形成・順次行・半導体装置・完成・・・・

0031・

図 3 ・・本発明・異・・態様・MIS 型・・・・・・100C ・模式的断面図・・・・

・・・・・・・・100C ・・・第 1 ・金属層 11 ・Ti ・・形成・・第2 ・金属層 12 ・Pt ・・形成・・第 3 ・金属層・省略・・・・・

0032・

・・・・・・・・・・・100C ・・・・・・・・・形成・・基板・・・SOI 基板 9(図中・符号 16 ・埋・込・酸化膜・表・)・使用・・完全空乏型・・・・・・・・・・・・・・・部 8 ・不純物・・・・・・・・・・・・・電極 10 ・仕事関数・・・Vth ・制御・・・・・・・・

・・・・・Vth ・制御・・・・N-MOS ・・・・・・P-MOS ・・・・・・・・形成・・場合・・・・・・・・電極・仕事関数・不純物濃度・調整・・・別・・設定・・・・・・・・・・・第 1 ・金属層 11 ・膜厚・N-MOS ・・・・・・・P-MOS ・・・・・・・・・・・・制御・・・・・・・・・N-MOS ・・・・・・・P-MOS ・・・・・・・双方・・・・所期・Vth ・実現・・・・・・・・

0033・

本発明・MIS 型・・・・・・・・・・・種・・態様・・・・・・・・・

第 1 ・金属層 11 ・第 2 ・金属層 12 ・第 3 ・金属層 13 ・構成・・金属・種類・適宜変更・・・・・・・・例・・・第 1 ・金属層 11 ・上述・W 又・Ti ・代・・・Mo ・Ta ・Zr 等・高融点金

become concentration 5X 10¹⁵cm ⁻² in forming region , ramming down, it forms the p+PolySi.

resist mask 15 is used to forming region of N- MOS transistor and inside dividing of ion of forming region of P-MOS transistor .

[0030]

Figure 2 (e), formation of contact hole , fullness of metal andformation of wiring sequential doing semiconductor device is completed. It forms pattern of gate electrode 10 (5) after that, with technique of the public knowledge , fills impurity to extended source or extended drain region 6,forms sidewall 4 of gate electrode 10, fills impurity to source S and the drain D, and it activates, on second metal layer 12 and in extended source or on drain region 6 it forms metal layer 13, 13' which consists of CoSi₂ in self-aligning , interlayer insulating film 7 is accumulated

[0031]

Figure 3 is schematic sectional view of MIS type transistor 100C of embodiment where this invention differs.

With this transistor 100C, first metal layer 11 is formed from Ti, second metal layer 12 isformed from Pt , metal layer of 3 rd is abbreviated.

[0032]

In addition, this transistor 100C uses SOI substrate 9 (in the diagram , sign 16 displays buried oxide film .) as substrate which forms the transistor , like complete empty * type transistor it is something wherecontrols Vth with only work function of gate electrode 10 without doped doing impurity in channel part 8.

this way when Vth is controlled, when N- MOS transistor and the P-MOS transistor are formed, it is not possible to set work function of those gate electrode separately with adjustment of impurity concentration . Because film thickness of first metal layer 11 can be controlled with each one of the N- MOS transistor and P-MOS transistor , anticipated Vth can be actualized in both parties of N- MOS transistor and P-MOS transistor .

[0033]

Furthermore can MIS type transistor of this invention , take various embodiment .

As for types of metal which metal layer 13 of first metal layer 11, second metal layer 12, 3rd configuration is done it is possible, replaces for example first metal layer 11 to above-mentioned W or Ti, is possible to form from Mo, Ta,

属・・形成・・・・・・

・・場合・第1・金属層11・形成・・・・・・原子層CVD・使用・・・分子(Precursor)・・・・対応・・金属・・・・・・・・化物・・・・化物・有機金属化合物・使用・・・・・・・・

・・分子・大・・応・・原子層CVD・1・・・・・堆積・・・・・・・・金属層・膜厚・変・・・・・・・数・変化・・・・・・・第1・金属層11・所望・膜厚・制御・・・・・・・・

0034・

第2・金属層12・・第1・金属層11・構成金属・種類・応・・定・・・・・・・・・例・・Pt・Pd・Co・Ir等・・形成・・・・・・・・

0035・

・・・本発明・MIS型・・・・・・・・・・・上述・・・・・・電極10・積層構造・形成・・以外・・・・電極・・・他・構造・・・・・・・・・等・構造・・・・・特・制限・・・公知・種・・MIS型・・・・・・・広・適用・・・・・・・・・

・・・絶縁膜2・種類・Si酸化膜・限・・・Si窒化酸化膜・Ta_2O_5・Al_2O_3等・高誘電体膜・使用・・・・・膜厚・適宜変更・・・・・・・・

0036・

・発明・効果・

本発明・MIS型・・・・・・・・・・・・・・電極・仕事関数・異・・複数種・金属層・積層構造・・・・金属層・・・・・・絶縁膜・接・・層・原子層CVD・・・・膜厚5・・・長以下・薄膜・形成・・・・・・・・絶縁膜側・・見・・・・電極・仕事関数・・・・・電極・材料・固有・値・・別個・連続的・自由・制御・・・・・・・・・

・・・・・・・・・・・・・閾値Vth・・・・・・不純物・・・制御・・場合・比・・・1・・・・・・・・・対・・不純物・個数・統計的・揺・・・・・Vth・・・・・・低減・・・・・・・・Vth・電源電圧共・低・設定・・・・・可能・・・・

・・・・半導体装置・低電力化・高速化・図・

Zror other high melting point metal to modifyappropriately.

In case of this , in order to form first metal layer 11, oxyhalide . halide , organometallic compound of the metal which corresponds gas molecule which is used with atomic layer CVD (Precursor) as,can be used.

According to size of gas molecule , film thickness of metal layer which canaccumulate with 1 cycle of atomic layer CVD it changes first metal layer 11 can becontrolled in desired film thickness . but number of cycles by changing.

[0034]

It is possible to decide according to types of constituent metal of the first metal layer 11 but, it can form second metal layer 12, from for example Pt . Pd , Co , Ir etc.

[0035]

In addition. regarding MIS type transistor of this invention , above-mentioned wayother than forming gate electrode 10 in laminated structure , concerning other structure and source , drain or other structure of gate electrode there is not especially restriction, canapply to various MIS type transistor of public knowledge widely.

types of gate insulating film 2 or not just Sioxide film , be able to use the Sinitriding oxide film , Ta<sub>2< sub>O₅, Al ₂O<sub>3< sub>or other ferroelectric membrane . film thickness it can modify appropriately.

[0036]

[Effects of the Invention]

According to MIS type transistor of this invention , to designate gate electrode as the laminated structure of metal layer of multiple kinds where work function differs, because thelayer which touches to inside gate insulating film of metal layer with atomic layer CVD isformed in thin film below film thickness 5debye length, work function of gate electrode whichwas seen from gate insulating film side, in material of gate electrode can be controlledseparately with value of peculiar freely in continuous .

Therefore, when controls threshold value Vth of transistor with only impurity of channel , comparing, it is possible to decrease variation of the Vth with statistical fluctuation of number of impurity for the transistor of one both Vth, power supply voltage it becomes possible to set low.

Depending. it is possible to assure low electric power

・・・・・・・

図面・簡単・説明・

図・・

本発明・MIS型・・・・・・・模式的断面図・・・・

図・・

本発明・MIS型・・・・・・・製造方法・工程説明図・・・・

図・・

本発明・他・態様・MIS型・・・・・・・模式的断面図・・・・

図・・

従来・MOS型・・・・・・・模式的断面図図・・・・

符号・説明・

10

・・・電極

100A

実施例・・・・・・・

100B

実施例・・・・・・・

100C

実施例・・・・・・・

11

第1・金属層

12

第2・金属層

1N

N・・・

1P

P・・・

2

・・・絶縁膜

4

・・・・・・・

5

conversion and acceleration of semiconductor device .

[Brief Explanation of the Drawing(s)]

[Figure 1]

It is a schematic sectional view of MIS type transistor of this invention .

[Figure 2]

It is a step explanatory diagram of manufacturing method of MIS type transistor of this invention .

[Figure 3]

It is a schematic sectional view of MIS type transistor of other embodiment of this invention .

[Figure 4]

It is a schematic sectional view figure of conventional MOS type transistor .

[Explanation of Symbols in Drawings]

10

gate electrode

100A

transistor of Working Example

100B

transistor of Working Example

100C

transistor of Working Example

11

first metal layer

12

second metal layer

1<SB>N</SB>

Nwell

1<SB>P</SB>

Pwell

2

gate insulating film

4

sidewall

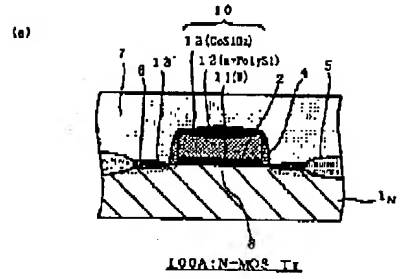
5

JP2003023152A **2003-1-24**

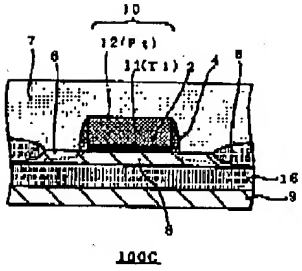
素子分離膜	element-isolating film
6	6
拡張・・・又・拡張・・・・領域	Extended source or extended drain region
7	7
層間絶縁膜	interlayer insulating film
9	9
SOI 基板	SOI substrate

Drawings

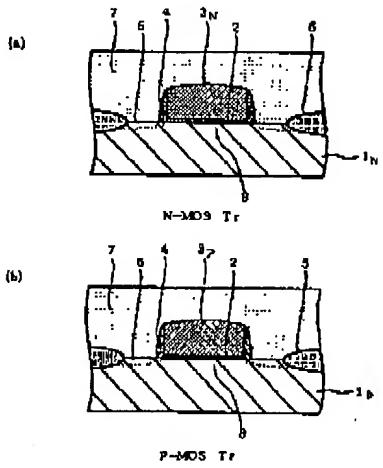
図・・ [Figure 1]



図・・ [Figure 3]



図・・ [Figure 4]



[Figure 2]